MATCHED FILTER AND SPREAD SPECTRUM RECEIVER

BACKGROUND OF THE INVENTION

The invention relates to a matched filter, a spread spectrum receiver and particularly to the correlation of a reference signal and a signal incoming to the receiver.

A spread spectrum system is a telecommunications system in which the bandwidth used for transmitting a signal is substantially wider than is required for the data to be transmitted. The spectrum of the signal is spread in a transmitter by means of a pseudo-random spreading code, which is independent of the original data. In direct sequence spread spectrum systems (DS-SS), a spectrum is spread to the available bandwidth by shifting the phase of the carrier in accordance with a pseudo-random spreading code. The bits of a spreading code are usually called chips as distinct from actual data bits.

Figure 1 shows a block diagram illustrating a direct sequence-based spread spectrum system. In the system, a signal of a data source 1-2 is first modulated in a data modulator 1-4 of a transmitter 1-1, whereupon a complex 1-6, 1-8 signal outcoming from the modulator 1-4 is modulated by multiplying said data modulated signal by a complex 1-12, 1-13 spreading code generated by a code generator 1-10 in a multiplier 1-14. A spreading code modulator 1-16 spreads the spectrum to be transmitted by means of the spreading code. A carrier generated by a high-frequency oscillator 1-20 is then modulated in a multiplier 1-18 by said data and code modulated signal, and an imaginary part 1-22 is removed from the signal to be transmitted. The transmitted signal propagates from an antenna 1-24 in the transmitter over a transmission path 1-26 to an antenna 1-32 in a receiver 1-30. In the receiver 1-30, a front end filter 1-34 separates an information signal from the entire frequency spectrum. A complex 1-35, 1-36 signal is mixed to a lower frequency by multiplying the signal by a complex 1-42, 1-44 signal generated by a voltage-controlled oscillator 1-40 in a multiplier 1-45.

In the receiver of a spread spectrum system, a reference signal, a code replica, which is an identical copy of said spreading code, is used in a despread modulator (spreading code demodulator) 1-48 to narrow the spectrum of an incoming signal. In Figure 1, a code generator 1-46 generates said spreading code replica, which is correlated in a multiplier 1-50 with a received signal by said spreading code replica. If the code replica and the received

code are the same and in phase, they correlate, and the transmitted data modulation can be restored to what it was before spreading. At the same time, different spurious signals are also spread. A band-pass filter 1-52, succeeding the despread modulator 1-48, lets the data modulation through, but removes

5   most of the power of a spurious signal, which improves the signal-to-noise ratio of the received signal.

In order to enable the detection of transmitted data in a spread spectrum receiver, the code replica generated by the receiver has to be synchronized (acquisition) with the received code as accurately as possible, and

10   said synchronization has to be maintained (signal tracking). The spreading code replica generated in the receiver thus has to be and stay in phase with the spreading code included in the received signal. For this reason, a special synchronization algorithm or unit is required for code synchronization, in addition to regular carrier and data synchronization. The speed of the acquisition,

15   i.e. the time taken by the code replica to hit the right phase with the received code, is an important performance parameter of a spread spectrum system. Many methods have been developed for the acquisition, in addition to which the system may comprise different aids for the acquisition that are related to the transmitted signal.

20   Matched filters are devices whose output is a time-reversed replica, a copy of the desired incoming signal, when the input is an impulse. Thus the transfer function of a matched signal is a complex conjugate of the signal matched thereto. A matched filter can be implemented to operate either continuously or discretely. A matched filter calculates the correlation between a

25   known reference signal and the signal to be measured, and gives a maximum output when the reference signal best corresponds to the incoming signal. For this reason, a matched filter is usable in signal acquisition in spread spectrum systems for searching for the right phase of the reference signal generated by a receiver. A matched filter may be shown to be the optimal way to identify

30   signals from AWGN (Additive White Gaussian Noise) type of noise.

Figure 2 shows a signal flow diagram of a feasible implementation of a matched filter. It consists of a delay line having intermediate outputs and of a passive filter matched to the waveform of a PRN (Pseudo Random Noise) chip. The output of the filter is matched to the basic pulse form of PRN

35   spreading bits. In Figure 2, in(n) represents a signal incoming to a filter and in(n-1), in(n-2) ... in(n-N_{MF}+1) represent an incoming signal delayed by 1,2 to

N_{MF}+1 delay elements Tc. c(0), c(1) ... c(N_{MF}-1) represent coefficients by which the incoming signal, delayed in different magnitudes, is multiplied. After the multiplication, the signals are summed up in an adder 2-10 and the sum signal is filtered in a filter 2-20.

5   The use of a matched filter in the synchronization of spread spectrum systems is known for example from 'Spread Spectrum Communications Handbook', Marvin K. Simon et al., McGraw-Hill, 1994, pages 815 to 832. In a known matched filter, the filter is matched to one received signal at a time. This requires either the use of several matched filters or the search for one

10   signal at a time, should the intention be to search for more than one signal.

When a band-pass type of signal is searched for with a matched filter from a received noisy signal, in known solutions the signal coming to the matched filter is pre-processed by multiplying it by a carrier estimate, which removes the frequency offset of the receiver. If the frequency offset is not

15   known, the signal has to be searched for at different frequency offsets over the entire frequency inaccuracy range. Furthermore, a matched filter searches for the right phase of the reference signal generated by a receiver. A matched filter calculates the correlation between a known signal and the signal to be measured, i.e. generates a measure for the identity of the two signals. The

20   outputs generated by the filter are typically non-coherently detected amplitude values.

Said measure is then compared with a set threshold value in order to decide if the two signals are in sync. In the simplest case, exceeding the threshold value means that the signal corresponding to the reference signal

25   has been identified and that the spreading code of the identified signal is in phase with the reference signal. This information serves to initiate actual signal tracking and reception. If no identification occurs (the threshold value is not exceeded), the acquisition system changes the phase of the locally generated reference code or changes reference signals, whereupon the correlation is

30   repeated. This continues until identification and synchronization are achieved, i.e. the reference signal corresponds best to the incoming signal. In this case the filter yields a maximum output. The tracking algorithm of the received signal is then initiated.

Since in the acquisition system, a band-pass type of signal is

35   searched, the matched filter has to be implemented either as a band-pass or an equivalent low-pass filter version. A low-pass type of acquisition system

using a matched filter is shown in Figure 3. Therein, a signal 3-1 incoming to identical, matched filters 3-10, 3-12 is divided into two parts, I and Q branches (I stands for In-phase, Q for Quadrature), and a signal that is generated by a local oscillator 3-2 and whose frequency can be substantially equal to the sum

5   of the intermediate frequency of the receiver and the Doppler frequency of the received signal is used to multiply a signal of the 3-I branch in a multiplier 3-6. Before a signal of the 3-Q branch is multiplied in a multiplier 3-8, the phase of a signal generated by the local oscillator is shifted 90 degrees in a phase inverter 3-4.

10   After the multiplication of the incoming signal, signals incoming from 3-I and 3-Q branches are correlated in substantially identical matched filters 3-10 and 3-12 with a code replica generated in the receiver. The signals outcoming from the matched signals are then detected, i.e. the signals of both branches are squared in elements 3-14 and 3-16, and the squared signals are

15   summed up in an adder 3-18 to obtain the square of the absolute value of a complex ingoing signal. A threshold value detector 3-20 then compares the value of the detected signal with a preset threshold value, a reference value. In the simplest case, exceeding the threshold value means that a signal corresponding to said reference signal has been detected and its spreading code is

20   in phase with the stored reference signal. The information is used to initiate actual signal tracking and reception.

In the structures of generally known matched filters, the timing of a reference signal and an incoming signal is fixed at the planning stage, and cannot thus be adjusted accurately for different timings. This causes problems

25   for tracking signals having a low signal-to-noise ratio, since the integration time required by them is long. This, in turn, requires accurate timing in the sampling of a matched filter, since the operation of a matched filter is subject to its reference signal being of the same length as a received signal in the time domain. In systems, in which the movement of a transmitter and receiver with

30   respect to one another is fast, a Doppler shift, whose magnitude depends on the frequency of said signal component, is created in the carrier and the spreading code. Since the frequency of the spreading code depends on the Doppler shift, the frequency is not always exactly the same. This should also be accounted for in the acquisition system if the required integration time (T_i) is

35   long. If the inaccuracy of the frequency exceeds $1/T_i$, the timing of the code changes more than one chip during integration, which prevents the acquisition

system from operating.

The integration time of a DS-SS acquisition system is also limited by the modulation of the transmitted data. Generally, the integration cannot be continued over a transmitted data symbol unless the modulation can be compensated for before the integration. For example in the widely used BPSK modulation (Binary Phase Shift Keying), a change in a data bit causes a 180° phase change in the signal, corresponding to an inversion in its sign. This is why the integration over a data bit causes significant degradation to the signal. Consequently, when the integration time is longer than the length of a data symbol, coherent integration can no longer be used. The use of non-coherent integration only is not feasible, since non-coherent detection weakens the signal-to-noise ratio if the incoming signal-to-noise symbol is initially negative.

A pass-band or low-pass type of matched filter can be implemented either as analog or digital. The most usual way is to implement matched filters based on the analog technology, wherein the delay line is implemented by SAW (Surface Acoustic Wave) or CCD (Charge Coupled Device) technologies. However, at the manufacturing stage, said systems are built for only a given reference signal. The delay line of an analog discrete-timed matched filter can be implemented for example based on the SC technology (Switched Capacitor). However, a problem in this technology is aliasing, for example.

The advancement of the digital technology has also brought about digitally implemented matched filters. To implement the required rapid summing up of many values is difficult in a digital filter. In a matched filter, stored signal samples, multiplied by the reference signal along the length of the filter have to be calculated to generate one outcoming sample. Conventionally, this has been accomplished by summing up a small number of numbers at a time and by repeating the process during several clock cycles. This avoids the implementation of a multiple-input adder.

BRIEF DESCRIPTION OF THE INVENTION

The object of the invention is a novel matched filter.

This object is achieved with a matched filter for implementing the correlation of an input signal and a reference signal, the filter comprising:

N parallel M-sample long shift registers for receiving an equal number of input signals at the sampling frequency of the input signal, wherein $N \geq 2$;

first means for storing K M-sample long reference signals, wherein

$K \geq 1$;

multiplexing means for applying one input signal and one reference signal at a time from said shift registers and said storage means to correlation calculation means by applying alternately at least one combination of the input

5 signals and the reference signals;

calculation means for calculating the correlation time-dividedly for each combination of an input and reference signal so that correlation results calculated from different signals appear at the output of the calculation means as a sequence.

10 Another aspect of the invention is a filter for implementing the correlation of an input signal and a reference signal, the filter comprising:

an M-sample long shift register for receiving an input signal at the sample frequency of the input signal;

first means for storing K M-sample long reference signals, wherein

15 $K \geq 2$;

multiplexing means for applying one input signal and one reference signal at a time from said shift registers and said storage means to correlation calculation means by applying alternately at least one combination of the input signal and the reference signals;

20 calculation means for calculating the correlation time-dividedly for each combination of an input and reference signal so that correlation results calculated from different signals appear at the output of the calculation means as a sequence.

Still another aspect of the invention is a spread spectrum receiver

25 comprising a device for detecting a demodulated signal, received by the receiver and converted into digital samples, the device comprising a matched filter for calculating the correlation between the input signal and at least one reference signal, and a controller for comparing the correlation results generated by the matched filter with a predetermined threshold value to determine if

30 a signal is found, said matched filter comprising:

N parallel M-sample long shift registers for receiving an equal number of input signals at the sampling frequency of the input signal, wherein $N \geq 2$;

first means for storing K M-sample long reference signals, wherein $K \geq 1$;

35 multiplexing means for applying one input signal and one reference signal at a time from said shift registers and said storage means to correlation

calculation means by applying alternately at least one combination of the input signals and the reference signals;

calculation means for calculating the correlation time-dividedly for each combination of an input and reference signal so that correlation results
5   calculated from different signals appear at the output of the calculation means as a sequence.

Yet another aspect of the invention is a spread spectrum receiver comprising a device for detecting a demodulated signal, received by the receiver and converted into digital samples, the device comprising a matched
10   filter for calculating the correlation between an input signal and at least one reference signal, and a controller for comparing the correlation results generated by the matched filter with a predetermined threshold value to determine if a signal is found, said matched filter comprising:

an M-sample long shift register for receiving an input signal at the
15   sample frequency of the input signal;

first means for storing K M-sample long reference signals, wherein K≥2;

multiplexing means for applying one input signal and one reference signal at a time from said shift registers and said storage means to correlation
20   calculation means by applying alternately at least one combination of the input signal and the reference signals;

calculation means for calculating the correlation time-dividedly for each combination of an input and reference signal so that correlation results calculated from different combinations appear at the output of the calculation
25   means as a sequence.

The invention is based on time-multiplexing in a matched filter at least two input signals to correlate with at least one spreading code or, alternatively, time-multiplexing at least two spreading codes to correlate with at least one input signal, allowing the same calculation capacity to be used for
30   several signals. Conventional matched filters are matched to one signal at a time, and therefore more than one filter has had to be used to simultaneously search for more than one signal to be received.

In a primary embodiment of the invention, an arithmetic unit comprises M multipliers, which multiply each sample in the shift register by a sam-
35   ple of a corresponding reference signal, and yield M results, and an adder means for summing up said M results to generate a correlation result at the

output of the filter, wherein M is the length of the filter. Such an arithmetic unit has to be able to very rapidly process a large number of numbers, wherefore it is difficult to implement. It is advantageous for the implementation if several matched filters are able to share this arithmetic unit.

5   The invention is suitable for digital implementations. The invention is particularly suitable for use in spread spectrum systems, which simultaneously use several spreading codes.

BRIEF DESCRIPTION OF THE FIGURES

The invention will now be described in greater detail by means of 10 preferred embodiments with reference to the attached drawings, in which

Figure 1 illustrates a direct sequence-based spread spectrum system;

Figure 2 shows a prior art implementation of a matched filter;

Figure 3 shows a low-pass type of acquisition system using a 15 matched filter;

Figure 4 illustrates the general architecture of an acquisition system of the spread spectrum receiver according to a primary embodiment of the invention;

Figure 5 is a block diagram illustrating data path pre-processing 20 blocks according to the primary embodiment of the invention;

Figure 6 is a block diagram illustrating a matched filter of a data path according to the primary embodiment of the invention;

Figure 7 shows a more detailed embodiment of the filter of Figure 6;

Figure 8 is a block diagram illustrating a data path search arithmetic 25 part according to the primary embodiment of the invention;

Figure 9 is a functional flow diagram of an acquisition system according to the primary embodiment of the invention;

Figure 10 is a state diagram illustrating a state machine according to the primary embodiment of the invention;

30   Figure 11 is a more detailed implementation of the pre-processing block of Figure 5;

Figure 12 is a block diagram of an integrate/dump filter;

Figure 13 is a block diagram of a numerically controlled oscillator; and

35   Figure 14 is a block diagram of an address generator.

DETAILED DESCRIPTION OF THE INVENTION

In the present document, a complex signal refers to a signal composed of two signal components, a real part and an imaginary part. Alternatively, the terms used are the I and Q branches or components of a signal (In-
5 phase and Quadrature). Amplitude and phase can be determined for a complex signal. Amplitude is obtained by using a mathematically defined absolute value operator for complex numbers. Phase can be calculated as a mathematically defined argument of a complex number.

An acquisition system according to a primary embodiment of the in-
10 vention implements K parallel channels time-divisionally. The limitation in the number of channels originates from the relation of the main clock frequency to the sampling frequency required by the matched filter. In the primary embodiment of the invention, this relation is $2 \cdot K$. A matched filter processes the In-phase (I) and Quadrature (Q) components of each channel, which decreases
15 the number of potential channels to the number K. If the number of potential channels is less than the total number (K_{TOT}) of spreading codes to be searched for, the spreading codes to be searched for are changed periodically in the primary embodiment of the invention. The reference signals corresponding to the spreading codes to be verified are located in a read-only
20 memory (ROM), and the reference signals are time-multiplexed by incrementing the address counter of said ROM. The counter counts from a basic address up to number K on the modulo-K_{TOT} principle, i.e. address 0 follows address K_{TOT}-1. The reference signals used are changed by changing this basic address, and this is done when all possible frequencies have been gone
25 through in a manner configured by the user. The basic address is changed as a configurable address addition, which is also calculable on the modulo-K_{TOT} principle. This adjustable basic addition allows the search process according to the search situation to be optimized.

Figure 4 shows the general architecture of the acquisition system
30 according to a primary embodiment of the invention. The acquisition system comprises four basic blocks: a data path block 4-1, containing the actual matched filter implementation; a control block 4-2 for generating the necessary control signals for the other blocks; a state machine 4-3 for controlling the search algorithm; and an I/O block 4-4 for connecting the matched filter to an
35 outer bus of the acquisition system. In the following, some of the blocks will be described in greater detail.

Data path block

The data path block is the core of the acquisition system. A matched filter is of the low-pass type, and the data path arithmetic is time-multiplexed to process both I and Q channels. In this implementation, the
5   length of the matched filter is M = N_{MF} samples.

The data path block of a matched filter comprises, not only the data path of the matched filter, but also blocks for processing an input signal. Figure 5 illustrates an implementation of the pre-processing stages of a data path block. In Figure 5, a sampled, complex signal 5-2 and 5-4 (I and Q compo-
10   nents), received from an RF front end and converted into digital is filtered in a low-pass filter 5-6 to prevent aliasing. The signal is then sampled at a frequency controlled by a numerically controlled clock oscillator (NCO) 5-8 in a decimation element 5-10, which generates processed samples at the sampling frequency of the matched filter. The sampling frequency of the input of the
15   matched filter is adjusted by means of the clock oscillator 5-8 so that the timing of the input signal corresponds to the timing of the samples of the reference signal.

After sampling, the samples are multiplied in a multiplier 5-12 by a complex carrier frequency replica generated by another numerically controlled
20   oscillator 5-14. The carrier frequency replica is of the form:

$$e^{j2\pi\omega_c n/F_s} = \cos(2\pi\omega_c n/F_s) + j \cdot \sin(2\pi\omega_c n/F_s)$$

wherein ω_c, n and F_s represent carrier frequency, sample number and sample frequency, respectively.
25   Thus the multiplication corresponds to rotating the phase of the input signal by the (estimated) carrier frequency. This multiplication may be also be implemented before re-sampling, should the frequency of the input signal exceed the sampling frequency of the matched filter.

Figure 6 shows the core block of a data path block, constituting an
30   actual matched filter 6-10. The samples generated from the input signal (for example in the pre-processing stages of Figure 5) are applied to said matched filter, which calculates their correlation with one or more reference signals. The filter comprises a number of parallel shift registers 6-22, one for each I and Q component of the signal. In the primary embodiment of the invention compris-
35   ing K separate channels, i.e. 2·K I and Q components, 2·K shift registers 6-22 are needed. Each incoming I or Q data stream 6-21 is applied to the corre-

sponding shift register 6-22, which is clocked at the code frequency or its multiple. The data stream applied to the shift register 6-22 is compared with reference signals stored in a memory 6-26, e.g. ROM or RAM (Random Access Memory). Signals to be compared time-dividedly are selected from the shift

5   register 6-22 and the memory 6-26, allowing the use of the same arithmetic part used for K channels, in accordance with the basic principles of the invention.

The input signal is selected with a signal multiplexer 6-24 and a selection signal 6-23, whereas the reference signal is selected from the memory

10   6-26 with a selection signal 6-25. In practice, the selection signal 6-25 can be a memory address. The memory addresses may have been created in an address generation unit, which applies read addresses synchronously to the read memory 6-26 in a manner to be described in connection with the state machine. This solution allows several spreading codes to be searched for in par-

15   allel by time-multiplexing the reference signals used. Consequently, the address 6-25 can be used to assign in the memory 6-26 the desired reference signal 6-27 for an input signal 6-20 selected with the selection signal 6-23. Alternatively, the memory 6-26 can be replaced with a reference shift register to which a reference signal generator applies the reference signal. The reference

20   shift register may be similar to the shift register 6-22.

The reference signal applied at each particular time from the reference shift register (or reference memory) 6-26 and from the data shift register 6-22, and the I and Q signals are multiplied by each other in a multiplier block 6-31. If both signals are composed of 1-bit samples, the multiplication may be

25   carried out for example with an XNOR gate whose output is 1 if its two inputs are equal. After this multiplication, there are N_{MF} data values 6-28.

Next, block 6-29 sums up all products of the multiplications for each sample to generate the final outputs of the matched filter. In the primary embodiment of the invention, this is implemented with an adder block, which cal-

30   culates the sum of all products during one clock cycle. In this connection, other summing methods may also be used.

An output 6-30 in the matched filter is composed of complex signals that correspond to the correlation of the input as a function of time. If the signal to be correlated is periodic and the length of period is N_C samples, periods of

35   N_C samples may be separated for each signal at the output 6-30, the periods corresponding to cross correlations having different phase differences. In the

case of a multi-channel (K channels) matched filter, outputs corresponding to the same phase difference of several channels (K) are in succession at the output 6-30.

Such a structure allows the outputs of K parallel matched filters to be calculated in succession, when the clock frequency used is 2·K times the sampling frequency of the incoming data.

Consequently, in a matched filter, stored signal samples of the length of the matched filter, multiplied by a reference signal, have to be calculated for one output. Conventionally, this is accomplished by summing up a small number of numbers at a time and by repeating the process during several clock cycles. This avoids the implementation of adders having a plurality of inputs. Known digitally implemented delay lines have also comprised only one reference signal, allowing only one signal to be correlated simultaneously with the same device. As described above, the present invention and its preferred embodiments allow easy, rapid and effective summing up of several values.

Figure 7 shows a more detailed block diagram of an implementation of the matched filter of Figure 6. For the sake of clarity, the embodiment is shown using four 6-sample long shift registers, four 6-sample reference signals and four multipliers. However, the filter can easily be extended to be suitable for any number of signals and register length.

Figure 7 shows four 6-sample shift registers 6-22 for receiving four input signals 6-21, each of the registers comprising stages 6-22A...6-22F (i.e. one stage per sample). The upper row in stages 6-22A...6-22F constitutes the first shift register, the second row the second shift register, etc. The selection signal 6-23 selects the row among the shift register stages 6-22A...6-22F that is applied as an output to the multiplier block 6-31 at each particular time. Code replicas (reference signals) are stored in a coefficient memory 6-26 composed of six four-location memory elements 6-26A...6-26F. The first row in the memory elements stores a first code replica, the second row a second code replica, etc. The selection signal 6-25 selects the row among the memory elements 6-26A...6-26F that is applied as an output to the multiplier block 6-31 at each particular time. The multiplier element 6-31 comprises 6 parallel multipliers 6-31A...6-31F. The first multiplier 6-31A of the multiplier element 6-31 multiplies the first sample (row in the register element 6-22A) of each input signal alternately by the first sample (row in the memory element 6-26A) of

each code replica. Similarly, the multiplier 6-31B multiplies samples obtained from the register stage 6-22B and the memory element 6-26B, etc. The signals multiplied in the multipliers 6-31A...6-31F are then summed up in the adder element 6-29. If the number of signals, i.e. channels, to be searched for at a

5   time is below the total number of spreading signals to be search for, the code replicas to searched for can be changed periodically. The code replicas can be stored for example in the ROM and they are time multiplexed by changing the memory address using for example a counter.

Figure 8 illustrates the last part of the data path block, the arithmetic

10   unit. The arithmetic unit calculates an estimate, in this case the square of the absolute value, of the absolute value of the complex output samples coming from the matched filter. Mathematically, this is performed by squaring the real and imaginary parts of a complex number and summing them up. The correlation results obtained from the matched filter (output 6-30 in Figure 6 or 7) are

15   applied to a register 6-41, which stores the results until they are squared in a block 6-42. The squaring block 6-42 takes one number and calculates its square. Squaring is performed separately for both I and Q components. The squares of the I and Q branches are then summed up in an adder 6-43. This yields the square of the absolute value of a complex input signal. The sum-

20   ming is performed the first time (squared sample of I branch) by summing up the result of the squaring with a zero obtained from the output of a multiplexer 6-44. The result is stored in a register 6-45. The second time (squared sample of Q branch) the result of the squaring is summed up with the output (squared sample of I branch) of the previous summing obtained via the multiplexer 6-44.

25   When the matched filter calculates the components (I and Q) of each complex sample in succession, the squares of the absolute values can be easily calculated by summing up the results of two successive squarings.

Finally, the sums are compared in a comparator 6-46 with a threshold value stored in a register 6-47, and the comparison result is applied via the

30   register 6-47 to the state machine 4-3 in Figure 4. To increase the probability of the right decision and to decrease the probability of wrong decisions, any exceeding of the threshold value levels must be secured by waiting for several comparison results corresponding to the same phase difference and reference signal. If sufficiently many comparisons exceed the threshold value level, the

35   signal can be declared found at good certainty. The state machine 4-3 implements a verification algorithm by means of which the threshold value level can

be lowered so low that even weak signals are found without wrong decisions being made on the finding of a signal. The obtained phase difference of the signal is used in the receiver to initialize a local reference code generator to the right phase.

5　　　　Since in a general case the frequency uncertainty of a receiver exceeds the total bandwidth ($1/T_i$) of the data path, a received signal has to be searched for using several frequency values. For this reason, the carrier frequency can be adjusted when the phase inaccuracy of the entire spreading code has been gone through.

10　　**State machine**

The state machine is responsible for higher-level signal search control of a matched filter MF. It implements K state machines operating in parallel, each of which is responsible for searching for one reference signal. The operations of state machine channels are independent of each other ex-

15　cept for changing the frequency of the carrier frequency replica, which always takes places only when each of the channels has processed all possible code phase offsets once. This means that some channels could search the code phase offsets at each frequency more than once and that the time between frequency sweepings depends on the slowest channel to check all code

20　phases.

In the primary embodiment of the invention, an acquisition system using the above matched filter can be controlled by the state machine 4-3 that attends to the implementation of the verification algorithm for phase differences that exceeded the threshold value comparisons and to the sweeping of

25　carrier frequencies for the search for several frequency offsets. Figure 9 shows an example of the functional flow diagram of a state machine and an acquisition system. In this example, the length of the filter is N_{MF} samples, and the acquisition system of the matched filter comprises K parallel time-dividedly separated channels.

30　　　　In step 9-2, one sample at a time of an input signal is loaded to a data register. Since the length of the matched filter is N_{MF} samples, $N_{MF}-1$ samples are loaded to the shift register. In step 9-3, still another new sample is loaded to the shift register, i.e. the last sample N_{MF} of the input signal. In step 9-4, the data in the shift register is compared with a code replica, i.e. a refer-

35　ence signal, which is a PRN type of signal. If the correlation does not exceed the set threshold value, the next sample of the input signal is loaded to the

shift register in step 9-3. In the simplest case, exceeding the threshold value means that the signal corresponding to said reference signal is detected and its spreading code is in phase with the stored reference signal. This information is used to initiate actual signal tracking and reception. However, if the

5 strength of the received signal is low as compared with noise, simply exceeding the threshold value is not sufficient to prove that the signal was found. For this reason, an algorithm can be used to verify the finding, whereby after the exceeding of the first threshold value a new input signal is loaded into the shift register and correlated with the reference signal with the matched filter in a

10 step corresponding to the point in time of the first finding.

Accordingly, if the reference value exceeds the set threshold value, the right phase of the code signal is potentially found, and the system transfers from signal tracking state 9-40 to a signal found verification state 9-50. Here, in step 9-6, the system first waits for N_{MF} samples, and then repeats the com-

15 parison in step 9-8.

If the value is less than the threshold value, the value of register *FAIL* is incremented by one unit in step 9-10, the next step being 9-12. Here, the value of the register *FAIL* is compared with a set maximum value, which indicates the allowed number of times below the threshold value. If the number

20 of comparison results below the threshold value exceeds a limit value set, the process returns to step 9-3. Otherwise, the next step is 9-6.

If the threshold value is exceeded, the value of register *DET* is incremented by one unit in step 9-14, the next step being 9-16. Here, the value of the register *DET* is compared with a set maximum value, which indicates

25 the allowed number of times the threshold value has to be exceeded before the signal can be declared found. If the number of comparison results exceeding the threshold value does not exceed a limit value set, the process returns to step 9-6.

The process continues as above until the number of samples ex-

30 ceeding or below the threshold value exceeds a preset, at least one number/threshold value. Then, in step 9-20, the signal can be declared found, or, alternatively, the search is continued from the next data sample in step 9-3.

Said signal search routine is executed independently for each reference signal. After all data samples of all parallel channels have been

35 checked, the frequency of the carrier replica oscillator is changed and the search process is repeated starting from step 9-2. When the search process is

repeated at all desired frequencies of the carrier replica oscillator, its frequency is zeroed and the search is repeated.

If generators tied down to one frequency reference generate the carrier frequency and the spreading code for a direct sequence system receiver, then the offset of the carrier frequency can also be used to calculate the required adjustment value for the sampling clock of the matched filter. Otherwise, the sampling frequency of a matched filter has to be adjusted with another algorithm. However, the Doppler shifts of the carrier and spreading code are directly proportional in relation to their frequencies.

Figure 10 shows the state diagram of a state machine controlling the search process according to the primary embodiment of the invention. The state machine has two active states and two states used for waiting. The initial state is an fwait state, in which new data is clocked to shift registers. In this state, waiting takes as many sample clock cycles as there are bits in the shift register, i.e. N_{MF} samples. Having waited for sweeping, the process enters the seek state. In this state, the output of the threshold value detector is checked for each sample, and if the threshold value is exceeded, the next state, verify wait, is entered, the DET counter is set to one and the FAIL counter to zero. If no exceeding of the threshold value occurred for any code offset (N_{MF} samples), the state machine sets a DONE flag for the current channel. Once all state machine channels are verified for each possible code phase offset, i.e. when all DONE flags are set, and all carrier frequencies to be searched have been gone through, the fwait state is re-entered.

In the verify wait state the state machine waits till completely new data is clocked inside the data shift register to improve the statistical quality of the detection, and a new comparison is carried out using the same code offset. To ensure signal detection, the threshold value comparisons are repeated several times in the same code offset state. After a wait of the length of a code (N_{MF} samples) in the verify wait state, the verify state is entered. In this state, the value of the threshold value detector is checked, and if detection is indicated, the DET counter is incremented by one. Otherwise, the FAIL counter is incremented by one. If the numbers of hits (DET) and failures (FAIL) are still below their maximum values, the verify wait state is re-entered. Otherwise, if the number of hits (DET) exceeds the maximum value, the signal is declared found and the current PRN code, frequency and code offset are given as the output of the acquisition system. After the last verification, there are two out-

comes. If the code offset is the last one, the frequency is changed and the fwait state is entered. Otherwise, the seek state is entered, and the search is continued as usual.

5   A state machine sweeps between the low and high limit values of a local oscillator frequency (LO) in configurable steps. The frequency range searched for is composed of a fixed intermediary frequency (IF) and a Doppler frequency. These limit values are set according to the actual RF (Radio Frequency) front-end intermediary frequency (IF) and the maximum expected Doppler shift. State machines also have a method of setting the acquisition
10   into its initial state. When a multi-channel matched filter is used, the state machine sees to it that the frequency search does not take place until all channels have once gone through all phase differences. In other respects, the different channels operate completely irrespective of each other. This ensures the best advantage obtained from parallelism.

15   **Pre-processing block**

Figure 11 shows a more detailed block diagram of the signal pre-processing block shown in Figure 5. An input signal i_in and q_in is decimated at ratio N_{DEC} in two integrate/dump filters 11-1 and 11-2. Figure 12 shows a more detailed block diagram of integrate/dump (ID) filters. The operation of the
20   filter is very simple. Data i_in enters a register 12-1, and its sign is then extended in block 12-2. The data is then applied to an adder 12-3, from the adder to a register 12-4 whose outputs are applied to a multiplexer 12-5 and to a holding register 12-6. Adder 12-3 sums up N_{DEC} samples incoming via the multiplexer 12-5 into a register 12-4 acting as an accumulator. The first sample of
25   the summing iteration is loaded directly to the accumulator 12-4 by adding 0 thereto (obtained from a second input of the multiplexer 12-5). In other iterations, the output of the multiplexer 12-5 is the output of the accumulator register 12-4.

Referring again to Figure 11, the outputs of integrate/dump filters
30   11-1 and 11-2 are applied to the multiplexer 11-3, which, according to its selection signal (din_sel) selects alternately one of the inputs as output, which is applied to the multiplier 11-4. To a second input of the multiplier is applied an output from the multiplexer 11-5, which, according to its selection signal (sin_cos_sel), selects from a sine/cosine table 11-6 a cosine output or a sine
35   output to be applied to the multiplier 11-4. Table 11-6 is controlled by a locally generated carrier replica phase signal ph_in. The adder 11-7 can alternatively

sum up the output of the multiplier and the output of the multiplexer 11-8 or subtract the output of the multiplier from the output of the multiplexer. The adder is controlled by a signal ena_sub. The output of the adder 11-7 is applied to an accumulator register 11-9, whose output is further applied to holding

5   registers 11-10 and 11-11 and to the multiplexer 11-8. Zero (0) is applied to a second input of the multiplexer 11-8 and it is controlled by a selection signal ena_add. The registers 11-10 and 11-11 give data outputs i_out and q_out, respectively.

The structure shown in Figure 11 is used to perform complex multi-

10   plication with carrier replica $\left(e^{j2\pi\omega_c n/F_s} = \cos(2\pi\omega_c n/F_s) + j\cdot\sin(2\pi\omega_c n/F_s)\right)$ in accordance with the following algorithm:

1. ACC =   i_in · cos(LO)
2. ACC = ACC + q_in · sin(LO) → i_out
3. ACC =   q_in · cos(LO)

15   4. ACC = ACC - i_in · sin(LO) → q_out,

Numerically controlled oscillator (NCO)

Figure 13 illustrates a numerically controlled oscillator. The NCO comprises a phase accumulator that accumulates frequency input values for

20   each sample. The accumulator is composed of an adder 13-1 and a register 13-2. The output of the register 13-2 generates a signal ph_out.

Address generator unit

Figure 14 shows the block diagram of an address generator unit of a code replica memory. The circuit comprises a basic register *base* 14-1, from

25   which an address is first loaded via multiplexers 14-2 and 14-3 to an address counter 14-4. The multiplexer 14-3 is controlled by a signal ena_conf. The value of the address counter 14-4 is incremented in a loop comprising an adder 14-5 and the multiplexers 14-2 and 14-3, until a signal zero_cnt, which controls the multiplexer 14-2, forces the value of the basic register 14-1 to be

30   loaded again to the address counter (*count*) 14-4. On the other hand, a loop comprising an adder 14-6 and a multiplexer 14-7 periodically increases the value of the basic register 14-1 when a control signal ena_base is set to one. The state machine 4-3 attends to this when all code replicas in the present group have been checked. The signal ena_base is applied to the basic regis-

35   ter 14-1 via an OR gate 14-8, whose second input is the signal ena_conf. The value for increasing the basic register 14-1 can be set by loading it to a regis-

ter *delta* 14-8.

Control block

A control signal for the data path 4-1 and the state machine 4-3 is generated in an MF control block 4-2 by decoding values 12-2, which are obtained from a counter 12-1 that counts from value 0 to value 2·K-1, as Figure 12 illustrates. This yields a sample rate, equal to the main clock divided by the value 2·K. Since the data path 4-1 processes K reference signals at the same time, it only has two clock cycles time to perform all operations. Chained, the total delay of the data path from the input of the shift register to the state machine is eight clock cycles. Input signal processing and data path operation are interleaved such that they both process data in parallel. The data path uses the inputs one sample later.

The operations required by the data path can be divided into three parts: during the first part, the I channel result is calculated, the Q channel result is then processed during the second part and added to the result of the I channel. Finally, the result is compared during the last part. All these operations can be interleaved by means of pipeline registers on the data path. The control signals for the data path are generated as a continuous stream except for two cases: start-up and re-synchronization. In these cases, the generation of the control signals is delayed by a time corresponding to the total pipeline delay of the components preceding said block.

As was described above, in the system and method of the invention and its preferred embodiments, the implementation of a multi-channel matched filter has been solved efficiently and in a manner that saves complex components.

It is obvious to a person skilled in the art that as technology advances, the basic idea of the invention can be implemented in a variety of ways. The invention and its embodiments are thus not limited to the above examples, but may vary within the claims.